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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,267	03/20/2001	Tyler Lowrey	2024.24	2620

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EXAMINER

CAO, PHAT X

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	09/813,267	Applicant(s)	LOWREY ET AL.
Examiner	Phat X. Cao	Art Unit	2814

^ The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 20 December 2002.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-44 is/are pending in the application.

4a) Of the above claim(s) 22-31 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-21 and 32-44 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____.
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) Other: _____

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I, claims 1-21 and 32-44 in Paper No. 11 is acknowledged.

Claim Objections

2. Claims 13 and 41 are objected to because of the following informalities: in claim 13 and claim 41, "less then" should be changed to "less than". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being

Art Unit: 2814

examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-2, 4-7, 9, 12, 15-16, 32-34, 36-37, 40, 43-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Doan et al (US. 6,423,621).

Doan (Fig. 13) discloses an electrically operated memory element, comprising: a programmable resistance memory material 120 made of chalcogenide (column 7, lines 59-61); and a conductive layer 102 having a tapered raised portion 114 extending from a linear edge of the layer 102 to an end adjacent the memory material 120, wherein the raised portion 114 (or a conductive sidewall spacer) is formed in a via having cylindrical sidewall surface (Figs. 4b and Fig. 22) or flat sidewall surface (Fig. 4a), and wherein all of the electrical communication inherently occurs through the top surface 118 of the raised portion 114 because the top surface 118 is in direct contact with the programmable resistance material 120.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2814

6. Claims 1-21 and 32-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Ovshinsky (US. 5,687,112).

Ovshinsky (Fig. 2) discloses an electrically operated memory element, comprising: a programmable resistance memory material 36 made of chalcogenide; and a conductive liner layer 34 having a tapered raised portion extending from a linear edge of the layer 34 (see "edge" labeled by the Examiner in Fig. 2) to an end adjacent the memory material 36, wherein the conductive layer 34 is disposed on the sidewall surface of the opening formed in the dielectric layer 18, and wherein all of the electrical configuration inherently occurs through the top surface 16 of the raised portion because the top surface 16 is in direct contact with the programmable resistance material 36. Ovshinsky further discloses that the cross-sectional area of the raised portion is less than 500 angstroms [$\pi \times (0.025 \text{ um}^2)$], and the conductive layer which are formed having flat peaks can be fabricated as conical, pyramidal, elongated or wedge-shaped flutums (column 14, lines 50-64).

7. Claims 1-4, 6-10, 12, 14-21, 32-33, 35-38, 40, and 42-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Ovshinsky et al (US. 5,414,271).

Ovshinsky (Fig. 1) discloses an electrically operated memory element, comprising: a programmable resistance memory material 36 made of chalcogenide; and a conductive liner layer (32,34) having a tapered raised portion extending from a linear edge of the layer (32,34) to an end adjacent the memory material 36, wherein the conductive layer (32,34) is disposed on the sidewall surface of the opening formed in the dielectric layer 20, and wherein all of the electrical

Art Unit: 2814

communication inherently occurs through the top surface or top edge of the raised portion because the top surface or top edge of the raised portion is in direct contact with the programmable resistance material 36.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 13 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan et al (US. 6,423,621).

Doan further disclose that the raised portion 114 of the conductive layer has an area of about 0.00785 um^2 (column 7, lines 27-30) or an area as small as possible as disclosed in Fig. 32 for maintaining uniformity and dimensional control (column 7, lines 30-34). From these teachings, it would have been obvious to one skilled in the art to form the contact area of the raised portion of Doan with the dimension as claimed (i.e., 0.005 um^2) for the reasons as suggested.

10. Claims 1-5, 7, 9, 11, 13-21, 32-37, 39, and 41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez et al (US. 5,854,102) in view of Doan et al (US. 6,423,621).

Art Unit: 2814

Gonzalez (Fig. 8) discloses an electrically operated memory element, comprising: a programmable resistance memory material 46 made of chalcogenide; and a conductive layer or a conductive sidewall spacer 38 in electrical communication with the memory material 46 and vertically disposed on the cylindrical sidewall surface of the opening (via) formed in the insulative layer 20, wherein all of the electrical configuration inherently occurs through the top surface of the conductive layer 38 because the top surface of the conductive layer 38 is in direct contact with the programmable resistance material 46.

Gonzalez does not disclose the conductive layer 38 having a raised portion extending from an edge of the layer to an end adjacent the memory materials.

However, Doan (Fig. 12) teaches the forming of the electrical contact 102 having a raised portion 114 in contact with a programmable resistance material 120. Accordingly, it would have been obvious to modify the electrical contact of Gonzalez by forming a raised portion with the structures as set forth above because according to Doan, such electrical contact would provide denser memory arrays and would minimize the power requirements for memory cells (column 3, lines 1-5).

Double Patenting

11. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible

Art Unit: 2814

harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

12. Claims 1-21 and 32-44 are provisionally rejected under the judicially created doctrine of double patenting over claims 84-100, 102-115, 117-131, 133-141, 143-157, 177-181, and 184-189 of copending Application No. 09/620,318. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: both applications claim a memory element comprising a conductive layer of chalcogenide in electrical communication with the memory material, wherein the

Art Unit: 2814

conductive layer having a raised portion extending to an end adjacent the memory material.

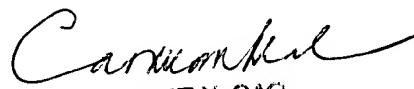
Moreover, the claims in the instant application are broader versions of the claim in copending application.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The Examiner can normally be reached on Monday through Thursday. If attempts to reach the Examiner by telephone are unsuccessfully, the Examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

PC
April 4, 2003


PHAT X. CAO
PRIMARY EXAMINER